From the latest ITRS -
Digital SOC IC Capability & Productivity:
ITRS - Figure [2]: The Design Productivity Gap

Potential Design Complexity and Designer Productivity

- Logic Tr./Chip
- Tr./S.M.

3 Yr. Design Staff

Year | Technology | Chip Complexity | Frequency | Staff | Staff Cost*
--- | --- | --- | --- | --- | ---
1997 | 250 nm | 13 M Tr. | 400 | 210 | 90 M
1998 | 250 nm | 20 M Tr. | 500 | 270 | 120 M
1999 | 180 nm | 32 M Tr. | 600 | 360 | 160 M
2002 | 130 nm | 130 M Tr. | 800 | 800 | 360 M

* @ $150K / Staff Yr. (In 1997 Dollars)
Figure [1]: Issues in IC Design

- Functional Design
- HW/SW Partitioning
- Logic Optimization
- Technology Mapping
- Analog Macro Design
- Design for Manufacturing
- Integrated flow/API
- Incremental optimization
- Param. Yield Optimization
- Mask Corrections
- Modeling tools

- Performance Modeling
- Power Estimation
- Power Estimation
- Statistical Process Modeling
- Failure Analysis

- System Simulation
- Functional Simulation
- Functional Simulation
- Process
- Masks
- Yield

- Test Architecture
- Test Logic Insertion (BIST)
- Test Model Generation
- Noise, Delay, Defect Tests
- Pattern Gen.
- Chip Test
- Diagnostics

- Logic and Interconnect Planning
- 3D Extraction
- Power, Noise
- Signal Integrity
- Circuit Simulation
- Layout Checking
- Equivalence Checking
- Dynamic Timing/SI Verification
Superexponentially Increasing Design Complexity

- Functionality + Testability
- Functionality + Testability + Wire Delay
- Functionality + Testability + Wire Delay + Power Mgmt
- Functionality + Testability + Wire Delay + Power Mgmt + Embedded software
- Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity
- Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity + Hybrid Chips
- Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity + Hybrid Chips + RF
- Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity + Hybrid Chips + RF + Packaging
- Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity + Hybrid Chips + RF + Packaging + Mgmt of Physical Limits
Many Industry Analysts now Stress that Analog Design Productivity needs to GROW in order to support the fast growing need for Analog SOC/DSP Chips!

But What will it take to **Greatly Increase** Analog Design Productivity?
Are Analog Design Productivity Issues the Same as ITRS Digital/SOC Issues?
Analog Design vs Increasing Design Complexity?

1 K

1 Billion

Functionality + Testability

Functionality + Testability + Wire Delay

Functionality + Testability + Wire Delay + Power Mgmt

Functionality + Testability + Wire Delay + Power Mgmt + Embedded software

Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity

Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity + Hybrid Chips

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Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity + Hybrid Chips + RF + Packaging + Mgmt of Physical Limits
## Analog Design vs Digital EDA Capabilities?

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- Functional Design
- HW/SW Partitioning
- Performance Modeling
- Power Estimation
- System Simulation
- Functional Simulation
- Formal Checking
- Test Architecture
- Test Logic Insertion (BIST)
- Test Model Generation
- Noise, Delay, Defect Tests, Pattern Gen.
- 3D Extraction
- Power, Noise, Signal Integrity
- Circuit Simulation
- Layout Checking
- Equivalence Checking
- Dynamic Timing/Signal Verification
- Process, Masks, Yield
- Chip Test, Diagnostics
- Param. Yield Optimization
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- Modeling tools
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